Amendments to the Specification:

Please amend page 11, paragraph 32 of the detailed description as follows:

[0032] FIG.5 illustrates a trellis encoder (28) and a precoder (27) used in the ATSC 8T-VSB transmission system (25) shown in FIG.3. They receive two input bits d0 and d1 and generate the corresponding output bits c0, c1, and c2. The 8T-VSB modulator (29) generates a modulation value (z) based on c0, c1, and c2. In FIG.5, 27a and 28b are adders, and ~~28b~~ 27b, 28a, and 28c are registers. As it is shown in the figure, the input bit d1 is precoded in the precoder (27) to become c2, and the input bit d0 becomes c1. In addition, the output bit c0 is determined based on the register values S0 and S1. Thereafter, the modulation value (z) of the 8T-VSB modulator (29) is determined based on c0, c1, and c2.